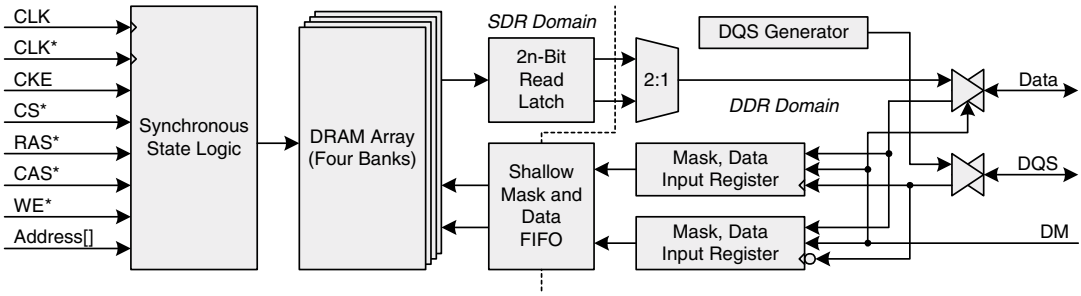

FIGURE 8.6 Basic DDR SDRAM architecture.

ble the speed of the control interface, because an SDRAM is almost always used in burst mode where the rate of commands is significantly less than the rate of data transferred.

The data interface contains a mask that has been renamed to DM and a new data strobe signal, DQS. DM functions as DQM does in an SDR device but operates at DDR to match the behavior of data. DQS is a bidirectional clock that is used to help time the data bus on both reads and writes. On writes, DQS, DM, and data are inputs and DQS serves as a clock that the SDRAM uses to sample DM and data. Setup and hold times are specified relative to both the rising and falling edges of DQS, so DQS transitions in the middle of the data valid window. DQS and data are outputs for reads and are collectively timed relative to CLK/CLK*. DQS transitions at roughly the same time as data and so it transitions at the beginning of the data valid window.

When reading, 2n bits are fetched from the DRAM array on the CLK domain and are fed into a 2:1 multiplexer that crosses the SDR/DDR clock domain. In combination with a DQS generator, the multiplexer is cycled at twice the CLK frequency to yield a double rate interface. This scheme is illustrated schematically in Fig. 8.7. Because DQS and data are specified relative to CLK/CLK* on reads, the memory controller can choose to clock its input circuitry with any of the strobe or clock signals according to the relevant timing specifications. Writes function in a reverse scheme by stacking two n-bit words together to form a 2n-bit word in the DRAM's CLK domain. Two registers are each clocked alternately on the rising and falling edges of DQS, and their contents are then transferred to a shallow write FIFO. A FIFO is necessary to cross from the DQS to CLK domains reliably as a result of skew between the two signals.

Tight timing specifications characterize DDR SDRAM because of its high-speed operation: a 333-MHz data rate with a 167-MHz clock is not an uncommon operating frequency. For reliable operation, careful planning must be done at the memory controller and in printed circuit board design to ensure that data is captured in as little as 1.5 ns (for a 333/167-MHz DDR SDRAM). These high-

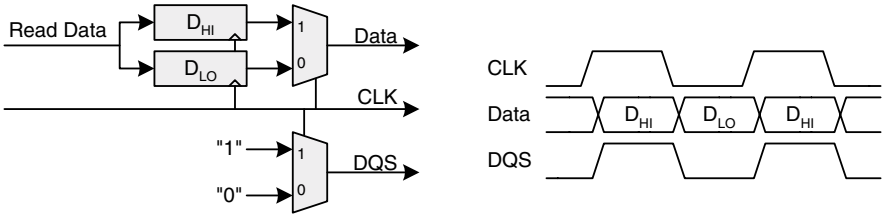

FIGURE 8.7 SDR-to-DDR data conversion scheme.

speed data buses are treated as *source-synchronous* rather than synchronous. A source-synchronous bus is one where a local clock is generated along with data and routed on the circuit board with the data signals. The clock and data signals are length-matched to a certain tolerance to greatly reduce the skew between all members of the bus. In doing so, the timing relationships between clock and data are preserved almost exactly as they are generated by the sending device. A source-synchronous bus eliminates system-level skew problems that result from clocks and data signals emanating from different sources and taking different paths to their destinations. Treating the DDR SDRAM data bus source-synchronously as shown in Fig. 8.7 guarantees that the data valid window provided by the driver will be available to the load. Likewise, because DQS is bidirectional, the SDRAM will obtain the same timing benefit when accepting write-data from the memory controller.

Methods vary across DDR SDRAM implementations. While the SDRAM requires a fixed relationship between DQS and data for writes, the memory controller may use either DQS or a source-synchronous version of CLK with which to time read data. DQS must be used for the fastest applications, because it has a closer timing relationship relative to data. The usage of DQS adds some complexity, because it is essentially a bidirectional clock. There are also multiple DQS signals in most applications, because one DQS is present for every eight bits of data.

Some applications may be able to use CLK/CLK* to register read data. The memory controller typically drives CLK/CLK* to the SDRAM along with address and control signals in a source-synchronous fashion. To achieve a source-synchronous read data bus, a skewed version of CLK/CLK* is necessary that is in phase with the returned data so that the memory controller sees timing as shown in Fig. 8.7. This skew is the propagation delay through the wires that carry the clocks from the memory controller to the SDRAM. These skews are illustrated in Fig. 8.8a, and the associated wiring implementation is shown in Fig. 8.8b. CLK´ and CLK´* are the clocks that have been skewed by propagation delay through the wiring. A source-synchronous read-data bus is achieved by generating a second pair of clocks that are identical to the main pair and then by matching their lengths to the sum of the wire lengths to and from the SDRAM. The first length component cancels out the propagation delay to the SDRAM, and the second length component maintains timing alignment, or phase, with the data bus.

With the exception of a faster data bus, a DDR SDRAM functions very much like a conventional SDRAM. Commands are issued on the rising edge of CLK and are at a single data rate. Because of the internal 2n-bit architecture, a minimum burst size of two words is supported. The other burst length options are four or eight words. To read or write a single word, DM must be used to mask or inhibit the applicable word. Two CAS latency options are supported for reads: 2 and 2.5 cycles. Two CL = 2 reads are shown in Fig. 8.9. DQS transitions from input (tri-state) to output one cycle (1.5 cycles for CL = 2.5) after the assertion of the read command. It is driven low for one full cycle (two DDR periods) and then transitions on each half of CLK for the duration of the burst, after which it

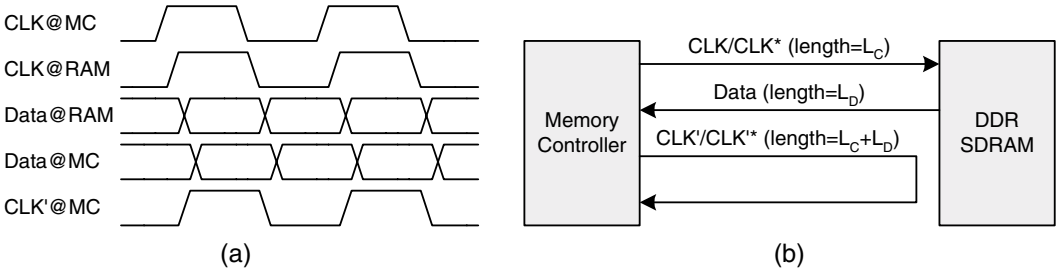

FIGURE 8.8 Source-synchronous read data with CLK/CLK*.